ABSTRACT OF THE DISCLOSURE

A semiconductor memory device comprises: a write data controller for receiving predetermined bits of data inputted through data input/output pins to generate plural bits of data, and a read data controller for serially converting the plural bits of data to generate serially converted data through one of the data input/output pins during a test operation; and the write data controller for receiving plural bits of data inputted through the input/output pins to generate the plural bits of data, and the read data controller for receiving the plural bits of data to generate the plural bits of data through the data input/ output pins during a regular operation, wherein the number of the plural bits is N times the number of the predetermined bits, N being a natural number.